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Application

For

United States Non-Provisional Utility Patent

Title:

10   **METHOD AND APPARATUS FOR EFFICIENT AND FLEXIBLE ROUTING**

BETWEEN MULTIPLE HIGH BIT-WIDTH ENDPOINTS

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METHOD AND APPARATUS FOR EFFICIENT AND FLEXIBLE ROUTING BETWEEN MULTIPLE HIGH BIT-WIDTH ENDPOINTS

Field of Invention

5   Invention relates to digital signal switching and routing, particularly to flexible

interconnection between multiple high bit-width endpoints.

Background of Invention

Conventional electronic systems, such as personal computers (PCs), provide signal

interconnections between various functional components or other system modules, such as

10   peripherals, storage, interfaces, or media devices. For example, so-called multi-media PC

and other related electronic hardware may provide multiple inputs and outputs for digital

audio data signal connections, whereby data signals are sent from certain input(s) to

certain output(s).

15   In some implementations, digital signal switching is accomplished using hardware-

based multiplexers, shared bus, or digital controller approach. Multiplexer approach,

however, typically requires relatively large number of gates or transistors, especially when

switching many endpoints, whereupon multiplexer size may grow linearly relatively to

number of switched signal lines. Moreover, shared bus approach faces challenge of

20   sending data simultaneously between multiple endpoint groups, since shared bus typically

restricts bus access to single group at a time.

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Furthermore, regarding digital controller approach to digital signal switching, hardware switching is typically achieved using relatively large temporary storage and so-called FIFO buffers at each input and output. In this way, digital controller effectively time-shares each channel and move data from one input FIFO to another output FIFO.

5   Such approach is undesirable, however, because FIFO buffers and digital controller require many gates to implement. Thus, there is a need for improved digital signal switching solution, particularly to provide flexible interconnection between multiple high bit-width endpoints.

Summary of Invention

10   Invention resides in apparatus and/or method for switching or routing digital signals flexibly through interconnection between multiple high bit-width endpoints. Multi-bit data signals are digitally switched between input and output endpoints for simultaneously interconnecting various sets of inputs and output endpoints. Single input may send data to single endpoint, or single input may send data to multiple output

15   endpoints. Multiple bitwidth data is serialized to single bitwidth at high data rate using N-by-1 multiplexer. Loadable barrel shifters shift serial data, so same data is used by multiple output endpoints at different times.

Brief Description of Drawings

20   FIGs. 1 and 2A-C are block diagrams of interconnect logic for implementing the present invention. FIGs. 3-5 are timing diagrams illustrating operational aspects of present invention.

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Preferred embodiment is implemented in circuit and/or operation thereof for selectably interconnecting electrical signals for transmission between specified endpoints.

5   Hence, multi-bit data signals are digitally switched, routed, or otherwise electronically communicated between one or more input and output endpoints, thereby simultaneously interconnecting various sets of inputs and output endpoints.

For example, present signal communication and processing implementation

10   operates such that single input may be caused programmably to send data signal to certain single endpoint, or such single input is caused to transmit data signal to multiple output endpoints. Furthermore, multiple bitwidth data is serialized in present embodiment to single bitwidth at high data rate using N-by-1 multiplexer, as described herein. In addition, loadable barrel shifters are provided for shifting serial data, such that same data

15   signal is used by multiple output endpoints, preferably at different times.

Generally, in accordance with one aspect of the present invention, incoming data signal may be received in substantially serial form, however, such serialized data signal may be provided effectively with one or more components or channels of data or other

20   representative signal information interleaved or otherwise encoded therein. Such serialized data signal may be convert into corresponding parallel-format signals, which represent such serial signal components or channelized data, preferably by using registers

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that latch parallel data, thereby using copies thereof for multiplexing operation to route received data signal.

Moreover, alternatively, incoming data signal may be received by present implementation in substantially parallel form, whereupon received parallel data signal may be converted substantially to serial form, preferably for signal communication and processing of high bitwidth data. Additionally, signal communication and processing may be performed upon received signal in serial form, preferably by using multiple copies of multiplexed signal.

As described further herein, barrel shifter or equivalent circuit functionality is provided in present implementation for interconnecting, switching, routing, or otherwise electrically coupling specified input data signal(s) to specified output data signal(s), or representative slots, ports, pins, locations, lines, or other electrically identifiable node, preferably at different times or clock cycles or periods.

Preferably, present implementation is provided on integrated circuit semiconductor chip wherein same set of input and/or output physical pins or endpoints are accessible for interconnection to one or more interface or protocol circuit, such as so-called AC97 or I2S coder/decoder (codec) functionality. Accordingly, present implementation serves generally as hardware block for controlling such serial interface or protocol, thereby enabling in- and/or out-bound serial data to be processed and switched in accordance with

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applicable codec configuration, signal interface, or other interface functional requirement. Hence, present implementation effectively avoids the need to use multiple sets of physical pins on-chip for such switch interface purpose.

5   In the case of media signal processing application, such as multi-track audio recording and playback equipment, interconnect or switching devices may be provided to enable flexible signal routing between multiple inputs and outputs connectors, thereby reducing device cost to implement flexible routing. Preferably, present interconnect scheme flexibly routes audio data, such as in so-called PCM format. Additionally, present 10   interconnect scheme may serve similarly to process other high bit-width digital data streams between multiple input and output endpoints.

Optionally, multiple sets of input and output signals and corresponding endpoints may be selectively interconnected using present scheme to enable simultaneous signal 15   communication, whereby each input and/or output endpoints are interconnected to transmit multiple bit-width data signals (e.g., for 32 bit-wide endpoints).

Generally, present interconnect scheme supports signal coupling to N-number of endpoints, such that each endpoint may send digital data signals to another endpoint. 20   Correspondingly, each endpoint may receive digital data signals from any other endpoints at any time. Preferably, data signal bitwidth of endpoints is larger than one bit.

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FIG. 1 block diagram shows an example of implementing present interconnect scheme for 4-way stereo input/output routing block 10, which couples to 4 serialized inputs (Inputs A-D) and 4 serialized outputs (Outputs A-D). Each serialized input is implemented into 2 distinct channels, and data are interleaved within the input signals.

5   Inputs are connected to two loadable barrel shifter modules (i.e., Input A is coupled to barrel shifters SH_A_left 12 and SH_A_right 14; Input B is coupled to barrel shifters SH_B_left 16 and SH_B_right 18; Input C is coupled to barrel shifters SH_C_left 20 and SH_C_right 24; and Input D is coupled to barrel shifters SH_D_left 26 and SH_D_right 28.)

In this interleaved manner, preferably for each input signal, left channel data is loaded into the first ("left") barrel shifter module, and right channel data is loaded into the second ("right") barrel shifter. Moreover, incoming serial data format can be either so-called I2S or AC97 convention. Optionally, input data may be received in parallel form

15   (i.e., not serialized), such that data is serialized prior to first before being received by routing block 10.

Output signals generated from each loadable barrel shifter module 12, 14, 16, 18, 20, 24, 26, 28 may be selectively interconnected to a set of M-to-1 1-bit-wide multiplexers

20   30, 32, 34, 36, where M represents total number of loadable barrel shifter modules. Multiplexers 30, 32, 34, 36 respectively generate Output signals A-D. Hence, any input channel may be routed electrically for signal transmission to any output channel, thereby

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minimizing gate usage. Note that number of input pins does not have to be same as number of output pins.

FIG. 2A shows general implementation of present interconnect scheme,
5 whereupon various endpoints 2(1-N) are flexibly switched and/or routed through hardware block 10. Preferably, improved endpoint is provided with serial to parallel converter circuits 6, which convert multi-bitwidth (e.g., 32-bits) signal for sending to or receiving from 1-bit wide signal generated by or transmitted by multiplexers in block 10.

10 When operating, present interconnect scheme may send data signal from one input endpoint to multiple output endpoints instead of one-to-one. Because output endpoints may need data from particular input endpoint at specified or different time, input data signal bits are serialized and saved effectively. To achieve such saving or storage approach, multiple sets of shift registers may be used for each input data, wherein each
15 shift register shifts at different times, depending on when corresponding output point needs data. However, multiple shift registers require many gates.

Hence, preferred interconnect scheme uses a set of loadable barrel shifter modules for each input endpoint. As shown in FIG. 2c, loadable barrel shifter module 9 is provide
20 such that serial input data is loaded into loadable barrel shifter 8 upon load enable signal being applied thereto. Specified single or multiple output multiplexers or endpoint(s) receive data signal at any time, independent of other output endpoints.

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Preferably, loadable barrel shifter module 9 includes single barrel shifter 8, wherein

shifter size equals bit-width of data format. For example, 24-bit data used for audio signal

processing application uses 24-bit barrel shifters. Barrel shifter is preferable over non-

5   barrel shifters, such that current data may be stored temporarily for use in next time slot.

Hence, in subsequent time slot, stored data may be reused for sending to another channel

or endpoint.

To illustrate present interconnect scheme, FIGs. 3-5 show timing cycles for routing

10   and/or switching data signals from stereo input to various multiple channels or outputs.

Generally, after received data signal is shifted to left output channel, such data is routed

back to applicable barrel shifter so that different channel may use the stored data. In

comparison, if shift registers are used, data is lost effectively after being shifted, and, thus,

2 sets of shift registers are required for each input channel in order to route subject data

15   signal to either left or right output channels. Accordingly, with barrel shifter approach,

each channel only needs one set of shifter, instead of two registers to hold same data.

FIG. 3 shows left and right interleaved components of Input #1 data stream timing

40 relative to Output #1 data stream 42, and Output #2 data stream 44. Here, stereo

20   input signal is interconnected to 2 stereo outputs simultaneously. FIG. 4 shows left and

right interleaved components of Input #1 data stream timing 46 relative to Output #1 data

stream 48, and Output #2 data stream 50, whereupon Output #2 is provided as left-

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repeated data stream. FIG. 5 shows left and right interleaved components of Input #1 data stream timing 52 relative to Output #1 data stream 54, and Output #2 data stream 56, whereupon Output #2 is provided as stereo-reversed output data stream.

5   Foregoing described embodiments of the invention are provided as illustrations and descriptions. They are not intended to limit the invention to precise form described. In particular, Applicants contemplate that functional implementation of invention described herein may be implemented equivalently in hardware, software, firmware, and/or other available functional components or building blocks. Other variations and

10   embodiments are possible in light of above teachings, and it is thus intended that the scope of invention not be limited by this Detailed Description, but rather by Claims following.

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